REMARKS

Re-examination and allowance of the present application is respectfully requested.

Initially, Applicants thank the Examiner for acknowledging their claim for foreign priority, and for confirming receipt of the certified copy of the priority document. Applicants also thank the Examiner for indicating consideration of all the documents cited in the Information Disclosure Statements filed on September 28, 2006, November 16, 2006, and August 1, 2007.

However, Applicants note that the Examiner has inadvertently failed to confirm the status of the filed drawings. Absent an express indication to the contrary by the Examiner in the next official communication, Applicants believe the submitted drawings to be accepted.

Claims 1-10 stand rejected under 35 U.S.C. §103(a) as being obvious over Japanese document JP 2003-223360 A, assigned to HITACHI, in view of HITACHI. Applicants respectfully traverse this ground of rejection.

According to a feature of the presently claimed invention, as defined by claim 1, an altering unit operates independently of an operation of a processor, and performs the altering while the cache memory is not accessed by the processor. According to another feature of the presently claimed invention, as defined in independent claim 8, the setting of the valid flag and the resetting of the dirty flag are performed independently of an operation of the processor, and are performed while the cache memory is not accessed by the processor. Applicants submit that at least these features, which are described at, for example, paragraph [0058] and [0059] of Applicants' specification, are neither disclosed or suggested by the applied art of record.

Applicants submit that HITACHI discloses the forcible resetting of a dirty flag in a cache entry after an address region is specified, using dedicated instructions such as a memory releasing instruction MREL and a dirty bit clearing instruction DCBDC.

In the instant invention, the altering unit performs the altering while the cache memory is not being accessed by the processor, by holding the command in a command holding unit pursuant to a normal data transfer instruction. Applicants submit that HITACHI fails to teach, let alone suggest, this feature. Applicants submit that HITACHI merely discloses operating a cache by a dedicated instruction, and that this differs from the presently claimed invention.

Furthermore, the altering unit operates independently of the processor in the current invention, as defined in independent claims 1 and 8. That is, the processor independently executes instructions once a command is stored in the command holding unit by the data transfer instruction. The altering unit alters the cache memory while the cache memory is not being accessed by the processor, independently of the processor. Thus, an additional instruction is not required, which simplifies operations. In a multi-threaded processor, associating a thread and a Way facilitates real time control. HITACHI teaches the use of dedicated commands, resulting in the addition of instructions for each Way in order to control the Ways separately. This is not practical. Applicants' solution, as described in independent claims 1 and 8, of holding a command in a register which can be accessed by the processor using a normal data transfer instruction produces an advantageous result in that by adding a register for each Way, no instructions need to be added. Further, since the altering unit rewrites a flag independent

of the processor by holding a command in a register, the valid flag and the dirty flag are rewritten at an appropriate timing, which prevents unnecessary replacing or write-back.

As discussed above, Applicants submit that HITACHI fails to disclose or suggest at least one of the valid flag and dirty flag being altered contrary to the state of the cache entry, independent of the operation of the processor, and while the cache memory is not accessed by the processor, by writing a command, by the processor, to a register that allows access from the processor using a data transfer instruction.

In view of the above, Applicants submit that the presently claimed invention is not obvious over HITACHI, either based upon its disclosure, or the "modification" set forth by the Examiner that "it would have been obvious to have used some buffer or register as a command holding unit." Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §103 rejection, and an indication of the allowability of the pending claims.

Further, Applicants submit new dependent claim 11 for the Examiner's consideration. Support for this feature may be found, *inter alia*, at paragraph [0045] of Applicants' specification. This claim specifies that the command holding unit includes a first field that specifies an operation to the valid flag, and a second field that specifies an operation to the dirty flag. Applicants submit that this feature is neither disclosed or suggested by HITACHI. Thus, Applicants submit that an additional ground exists for concluding that claim 11 is allowable over the applied art of record.

SUMMARY AND CONCLUSION

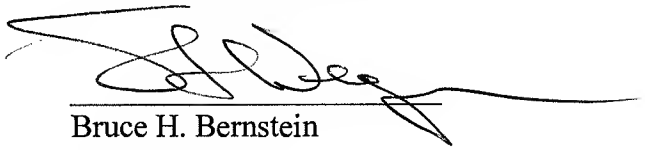
In view of the fact that none of the art of record, whether considered alone or in combination, discloses or suggests the present invention as now defined by the pending claims, and in further view of the above amendments and remarks, reconsideration of the

Examiner's action and allowance of the present application are respectfully requested and are believed to be appropriate.

Should the Commissioner determine that an extension of time is required in order to render this response timely and/or complete, a formal request for an extension of time, under 37 C.F.R. §1.136(a), is herewith made in an amount equal to the time period required to render this response timely and/or complete. The Commissioner is authorized to charge any required extension of time fee under 37 C.F.R. §1.17 to Deposit Account No. 19-0089.

If there should be any questions concerning this application, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Ryuta NAKANISHI et al.



Bruce H. Bernstein
Reg. No. 29,027

Steven Wegman
Reg. No. 31,438

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GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191